WHAT IS CLAIMED IS:

1. A memory apparatus formed on one semiconductor substrate, comprising:

a phase lock loop circuit, connected to receive a first clock signal having a first frequency, which generates a second clock signal which is substantially in phase with said first clock signal and has a second frequency;

a memory part which stores data; and

an interface circuit,

wherein said interface circuit in synchronism with said second clock signal, outputs said data.

2. A memory apparatus according to claim 1, wherein said memory part, responsive to said second clock signal, inputs an address.

3. A memory apparatus formed on one semiconductor substrate comprising:

a phase lock loop circuit, connected to receive a first clock signal having a first frequency, which generates a second clock signal which is substantially in phase with said first clock signal and has a second frequency;

a Random Access Memory (RAM); and

an interface circuit,

wherein said interface circuit in synchronism with said second clock signal, outputs data.

4. A memory apparatus according to claim 3, wherein said RAM, responsive to said second clock signal, inputs an address.

5. A memory apparatus formed on one semiconductor substrate, comprising:

a phase lock loop circuit, connected to receive a first clock signal having a first frequency, which generates a second clock signal which is substantially in phase with said first clock signal and has a second frequency;

a Read Only Memory (ROM); and

an interface circuit,

wherein said interface circuit in synchronism with said second clock signal, outputs data.

6. A memory apparatus according to claim 5, wherein said ROM, responsive to said second clock signal inputs an address.